To appear at the 30th IEEE European Test Symposium May 26-30, 2025, Tallinn, Estonia. ©IEEE

Computing with Printed and Flexible Electronics

Mehdi B. Tahoori*, Emre Ozer†, Georgios Zervakis§, Konstantinos Balaskas§, and Priyanjana Pal*
*Karlsruhe Institute of Technology, Karlsruhe, Germany,
†Pragmatic Semiconductor Ltd, Cambridge, UK,
§University of Patras, Patras, Greece
*{mehdi.tahoori, priyanjana.pal}@kit.edu, †eozer@pragmaticsemi.com, §{zervakis,kompalas}@ceid.upatras.gr

arXiv:2505.00011v1 [cs.AR] 21 Apr 2025

***Abstract*—Printed and flexible electronics (PFE) have emerged as the ubiquitous solution for application domains at the extreme edge, where the demands for low manufacturing and operational cost cannot be met by silicon-based computing. Built on mechanically flexible substrates, printed and flexible devices offer unparalleled advantages in terms of form factor, biocompatibility and sustainability, making them ideal for emerging and uncharted applications, such as wearable healthcare products or fast-moving consumer goods. Their desirable attributes stem from specialized fabrication technologies, e.g., Pragmatic's FlexIC, where advancements like ultra-thin substrates and specialized printing methods expand their hardware efficiency, and enable penetration to previously unexplored application domains. In recent years, significant focus has been on machine learning (ML) circuits for resource-constrained on-sensor and near-sensor processing, both in the digital and analog domains, as they meet the requirements of target applications by PFE. Despite their advancements, challenges like reliability, device integration and efficient memory design are still prevalent in PFE, spawning several research efforts towards cross-layer optimization and co-design, whilst showing promise for advancing printed and flexible electronics to new domains.**

I. Introduction

The continuous advancement of computing systems has made them an integral part of daily life, expanding in scale and impact with each technological breakthrough. For over five decades, silicon (Si)-based microprocessors have been the foundation of semiconductor technology, consistently improving in performance, area efficiency, power consumption, and cost. However, despite their relatively low unit cost of a few dollars, Si microprocessors face inherent evolutionary limitations that make them unsuitable for many emerging applications. These include fast-moving consumer goods (e.g., smart labels and packaging), wearable healthcare devices (e.g., smart patches and dressings), disposable medical implantables (e.g., neural interfaces), and diagnostic test strips (e.g., lateral flow tests). Such applications require not only extremely low costs but also flexibility, stretchability, and compact form factors–characteristics that conventional Si technology struggles to provide.

Printed and flexible electronics (PFE) emerge as a solution to address these limitations, offering unparalleled advantages in cost and form factor, to enable these emerging application domains. Silicon manufacturing comes with major operational, testing, and compliance expenses, whereas flexible integrated circuits (FlexICs) can be fabricated in smaller distributed facilities, with cheaper and even portable equipment, and without the need for protective packaging, thanks to their physical attributes [1]. Moreover, a key feature of PFE is sustainability. For example, the FlexIC process of Pragmatic Semiconductor, which is based on Indium Gallium Zinc Oxide (IGZO) thin-film transistors (TFTs), enables rapid production cycles while dramatically reducing environmental impacts–achieving a significant reduction in water usage, energy consumption, and carbon footprint [2]. Furthermore, their conformal, porous, and stretchable properties make printed and flexible technologies ideal for applications requiring physical flexibility and lightweight designs.

While printed and flexible circuits enable the development of ultra-low-cost and conformal hardware, they face significant challenges in achieving large-scale integration. These challenges originate from their relatively large feature sizes, limited device count and integration density, and high device latencies—several orders of magnitude below that of silicon-based VLSI [3], mainly stemming from their low-cost fabrication processes. Printed electronics technology is significantly slower (in the order of Hz) but enables in-situ tuning and point-of-use customization, while flexible electronics provide better performance (kHz range) and significantly higher integration density. Despite these limitations, PFE can meet the requirements of certain applications where performance and precision demands are minimal, such as circuits operating at low sampling rates (a few Hz) and limited bit precision [3]. As such, they are emerging as key enablers for computing in domains where conventional silicon systems have not yet achieved significant penetration.

Additionally, a key technological limitation is the lack of a robust p-type device in metal oxide, or a robust n-type one in organic electronic technologies. Consequently, printed and flexible circuits often rely on resistive-load configurations, such as resistor n-MOS designs. This poses significant constraints in low-power designs, as the use of resistive loads leads to higher power consumption, increased area requirements, and greater variability between devices compared to CMOS technology.

PFE may also be susceptible to aging-related degradation due to thermal stress over time, as well as process variations caused by manufacturing inaccuracies such as non-uniform device geometries and ink dispersion in printed electronics [4], [5]. Moreover, while they can resist mechanical stress, such as bending, without needing additional chip packaging like Si dies, they need to be validated, tested, and ensure operation under varying mechanical stress conditions like tensile and compressive modes [2]. These limitations also present substantial

Fig. 1: A flexible wafer on a polyimide substrate, and a FlexIC held in a tweezer

challenges in the design, reliability, and testing of printed and flexible circuits, thus necessitating novel *Design for Reliability (DfR)* solutions integrated in their design methodologies and complemented with post-manufacturing calibration and optimization.

Extensive research efforts have been dedicated to address the aforementioned challenges. This work presents the state-of-the-art in PFE, offering an overview from technology fundamentals and advancements, to practical applications, to novel design methodologies. Section II provides detailed information on emerging technologies and recent technological milestones. These include low-voltage, high-mobility Electrolyte-Gated FETs (EGFETs) enabling battery-powered operation [1], IGZO-TFTs on polyimide substrates supporting large-scale non-silicon microprocessors [2], and Pragmatic's FlexIC Gen3 platform showcasing mechanically robust submicron IGZO-TFTs on ultra-thin polyimide [6]. Section III focuses on application domains in which PFE insert intelligence at sub-cent costs, enabling affordable yet efficient computation at the extreme edge. In Section IV, several state-of-the-art design strategies for printed/flexible circuits are detailed, spanning from the digital to the analog domain. We focus on both general-purpose computing elements (e.g., flexible RISC-V microprocessors [2]), as well as domain-specific circuits which adopt high degrees of customization through bespoke and/or approximate designs. Bespoke circuits specifically leverage the low non-recurring engineering (NRE) costs of such technologies and tailor the circuit implementation to the application at hand, achieving impressive reductions in area, power and energy consumption, effectively enabling battery-powered operation. Section V presents an analysis of current efforts towards improving the reliability and robustness of printed and flexible devices and circuits, through fault sensitivity analysis, dedicated test generation methods, and robustness-aware training.

II. Technology and Fabrication

A. Pragmatic FlexIC Technology

Pragmatic's FlexIC technology uses an advanced process to fabricate physically flexible integrated circuits on a 200/300 mm polyimide wafers (see Fig. 1). The Gen3 FlexIC [6] is the latest platform that utilizes resistive n-type metal-oxide TFT technology, based on IGZO for production of FlexICs, by running several sequences of material deposition, patterning

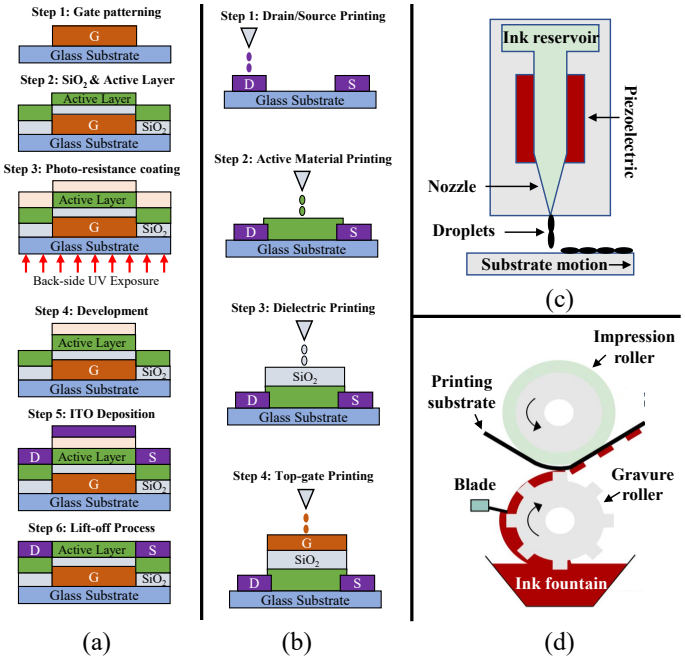

Fig. 2: Illustration of printed manufacturing techniques. (a) Subtractive and (b) additive processes, (c) inkjet and (d) gravure printing.

and etching. The Gen3 platform supports TFTs with a minimum channel length of 0.6 µm, and integrates key components such as resistors and capacitors. The polyimide substrate is ultra thin, with a thickness of less than 30 µm. FlexICs have demonstrated mechanical robustness with a radius of curvature as small as 3 mm without any damage to circuitry.

B. Printed Electronics

Printed electronics (PE) technology denotes a set of fabrication methods that leverage various printing techniques, including inkjet, screen, and gravure printing [17]. Optimal device performance in PE is traditionally achieved using vacuum-deposited highly purified molecular substrates. However, recent advancements in solution-based fabrication methods, such as spin-coating and inkjet printing, have attracted significant attention due to their potential for enhancing manufacturing efficiency and significantly reducing production costs. Printing technologies generally fall into two primary categories, illustrated in Fig. 2. First, replication printing techniques, such as gravure printing (Fig. 2(d)), are particularly suited for high-throughput, large-scale production. Second, jet printing methods, like aerosol or inkjet printing (Fig. 2(c)), cater to customized fabrication of electronic circuits in smaller, tailored batches. Furthermore, manufacturing approaches in PE can be classified as either subtractive or additive, shown in Fig. 2 (a) and (b), respectively. Subtractive manufacturing involves cycles of material deposition followed by selective etching, typically demanding specialized equipment and thus incurring higher costs. On the other hand, additive manufacturing sequentially deposits materials layer by layer to construct electronic components, a method clearly illustrated by inkjet printing. Although additive methods produce components with lower

TABLE I: Comparison of natively flexible general-purpose processors fabricated and validated

Features	PlasticCPU [7]	RFCPU [8]	Asynch. µproc. [9]	UHF RFCPU [10]	Organic µproc. [11]	Hybrid µproc. [12]	PlasticARM [13]	Flex6502-1 [14]	FlexiCore [15]	Flex6502-2 [16]	Flex-RV [2]
Data Bit-width	8	8	8	8	8	8	32	8	4 and 8	8	32
ISA	Custom	Custom	Custom	Custom	Custom	Custom	ARM	6502	Custom	6502	RISC-V
S: Synch. or A:Asynch.	S	S	A	S	S	S	S	S	S	S	S
CPU or SoC	CPU	SoC (ROM, RAM & RF Interface)	CPU	SoC (ROM, RAM & RF Interface)	CPU	SoC (CPU & ROM)	SoC (RAM, ROM & Peripherals)	CPU	CPU	CPU	SoC (Peripherals & ML Accelerator)
TFT Type	Poly-silicon	Poly-silicon	LTPS	Poly-silicon	Organic	Organic + Metal-oxide	Metal-oxide	Metal-oxide	Metal-oxide	LTPS	Metal-oxide
Technology Node (µ)	1.2	1	4	0.8	5	5	0.8	0.8	0.8	3	0.6
Logic Type	CMOS	CMOS	CMOS	CMOS	CMOS	Pseudo-CMOS	Resistive Load	Pseudo-CMOS	Resistive Load	CMOS	Resistive Load
Supply Voltage (V)	3.3	1.8	3.5-7	1.8	10	12	3-4.5	(2 & 3) or (3 & 6)	4.5	9	3
Clock Frequency (kHz)	10,000	3,390	30@3.5V and 500@5V	1120	0.04	2.1	29-40	10-71	12.5	454.5	60
Core Area (mm^2)	Not reported	196	156.25	93.45	33,700	22,600	59.2	24.91	5.56 & 6.06	75.33	17.5
Number of Devices	Not reported	71,000	32,000	133,000	3381	3504	56,340	16,392	2,104 & 2,335	12,628	∼38,000
NAND2-equivalent Gatecount	Not reported	17,750 (Estimated)	8,000 (Estimated)	33,000 (Estimated)	1127	876	18,334	2732	801	3200 (Estimated)	12,596
Power (mW)	Not reported	4.14	0.725@5V	0.81	0.092	Not reported	21	11.6-134.9	1.8 & 2.4	15.3	5.8
Year	2004	2005	2005	2008	2012	2014	2021	2022	2022	2024	2024

resolution and higher variability, their cost-effectiveness makes them highly appealing for various applications in PE. The minimal equipment requirements and the simplicity of maskless additive processes allow for the fabrication of extremely low-cost electronic circuits–sometimes costing less than a cent–at reduced development time [18].

In the respective literature, the printed EGFET technology [1] has attracted major interest. EGFET devices boast favorable mobility characteristics and operate at low supply voltages, as they are capable of functioning below 1V and even as low as 0.6V [19], aligning well with battery-powered printed applications.

III. Applications

PFE are specifically suitable for applications at the extreme edge for on-sensor and near-sensor processing, which is defined as the domain where the electronics deployed in an end device cannot be based on conventional Si technology because of one or more of these constraints: form factor, cost, conformability, biocompatibility and user comfort. An extreme-edge end device will need to process sensor data to extract knowledge, which typically involves predictions such as pattern recognition or classification.

Good examples of the extreme edge applications are logistics, fast-moving consumer goods (FMCG), healthcare wearables, implantable/ingestibles, textiles, agricultural and environmental monitoring. Smart packaging in the FMCG domain involves very cost-sensitive applications, where embedded electronics cannot cost more than a few cents. Making predictions is important for many FMCG applications, such as a smart package embedded with a flexible chip which can predict food freshness. Another example is an ECG patch or a smart dressing in healthcare domain, which requires conformable and comfortable electronics for patients. Such a patch or dressing–embedded with a flexible chip–can predict events like arrythmia/AF in the ECG patch, or healed wounds in the smart dressing. In the agricultural monitoring domain, a patch embedded with a flexible chip can be wrapped around a plant to monitor plant growth and predict growth anomalies.

IV. Computing Architecture

A. General-purpose Processors

Natively flexible general-purpose processors can be grouped into categories, based on the instruction set architecture (ISA) they follow, the utilized computational bitwidth and the semiconductor material with which they are developed. Early processors were 8-bit CPUs [7]–[10] with proprietary ISA, and developed using low-temperature poly-silicon (LTPS) TFT technology that has a high manufacturing cost and poor lateral scalability. An 8-bit arithmetic logic unit (ALU) with a print-programmable ROM was developed with metal-oxide TFTs, and was fabricated on polyimide [11], [12]. Flex6502 [14] was

an 8-bit processor in 6502 ISA-implemented and fabricated using IGZO-based FlexIC technology. Also, a low-temperature poly-silicon (LTPS) version of Flex6502 was fabricated and demonstrated [16]. FlexiCores [15] performed yield analysis of 4-bit and 8-bit processors in FlexIC technology.

PlasticARM [13] was the first 32-bit processor developed using flexible electronics technology. It was a system-on-a-chip (SoC) comprised of a 32-bit ARM CPU derived from the Arm® Cortex-M0+® processor supporting the Armv6-M architecture. It also integrated CPU peripherals, a ROM and a small latch-based RAM, all fabricated as a FlexIC. Flex-RV [2] was the first 32-bit RISC-V microprocessor in FlexIC, an important milestone in building ultralow-cost bendable computing architectures. Fabricated using 0.6 µm IGZO TFTs on a 30 µm polyimide substrate, Flex-RV is ultrathin, bendable, and sub-dollar in cost, making it ideal for low-cost, flexible electronics. It also supports ML workloads via an integrated programmable hardware accelerator, and runs at up to 60 kHz while consuming under 6 mW, maintaining functionality even under a 3 mm bending radius.

Table I shows the features and properties of the natively flexible general-purpose processors that have been fabricated and validated. The table does not include simulation-based printed and flexible processor studies that have not been fabricated and validated such as [1], [20].

B. Domain-specific Digital Processing Elements

Because of the highly embedded nature and short lifespan of many extreme edge applications, the development of domain-specific processing engines in PFE has emerged as the de-facto solution to address the inherent limitations in these technologies [21]. Available resources in printed and flexible circuits are very limited, typically constrained to only a few thousand gates [1], [22], [23]. Likewise, printed batteries can supply only a few tens of milliwatts of power [23], which is sufficient to drive, at most, a few thousand gates.

By leveraging the extremely low fabrication and NRE costs in PFE, high degrees of customization can be embedded within the circuit implementation, thus significantly reducing overheads associated with general-purpose functionality. Such customization levels are largely impractical in silicon technologies, due to the high costs of silicon process technology-including masksets and packaging costs.

In PFE, specialization is mainly enabled through alternative computing paradigms such as bespoke and approximate computing [24]–[33]. Bespoke circuits are highly customized and prioritize hardware efficiency over generalization capabilities [1], [21]–[23], [34], [35]. They also enable more compact designs with a reduced gate count, leading to lower marginal costs. Therefore, the bespoke design paradigm has not only gained significant traction in the development of complex systems, such as ML classifiers, for printed and flexible technologies, but has also emerged as the design standard due to its exceptionally high hardware efficiency.

1) Bespoke ML Classifiers: Printed and flexible ML represent an extreme subset within the TinyML domain where advancements have mainly been driven by bespoke ML circuits.

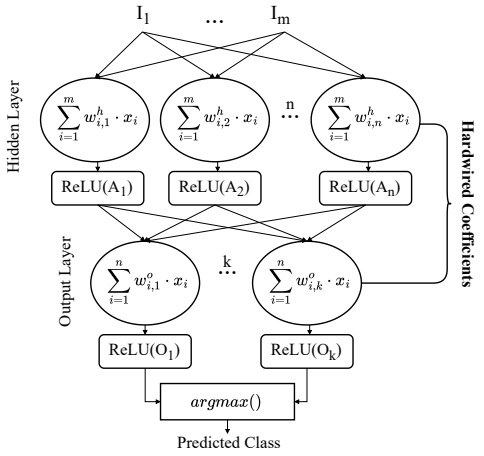

Fig. 3: Block diagram of fully-parallel bespoke MLP.

Bespoke classifiers are tailored to a specific model, trained for a given application and dataset. For instance, a bespoke ML engine would hardwire the trained parameters directly into the circuit implementation. In fact, the first flexible ML chips are designed and fabricated as FlexICs, following the bespoke design principal [34], [35]. Specifically, [35] implements a fully-parallel bespoke classification system as a FlexIC, whilst [34] is a flexible and hardwired binary neural network (BNN). Recently, arrWNN [36] has demonstrated a weightless neural network (WNN) implemented and fabricated as a FlexIC to detect arrhythmia events. An overview of existing printed and flexible bespoke ML classifiers is presented in Table II.

Studies like [24], [25], [37] have demonstrated that bespoke arithmetic units–such as multipliers with a hardwired multiplicand set to a specific constant–can be, on average, 5x smaller than their conventional counterparts. Additionally, embedding constants directly into the RTL description allows logic synthesis tools to propagate constants and further optimize logic downstream [23].

Most state-of-the-art domain-specific printed and flexible ML ASICs adopt fully parallel bespoke architectures, where model parameters are hardwired directly into the circuit design. These implementations are entirely combinational, meaning that the classifier's outputs update instantly in response to input changes. For instance, in a neural network [26], [33], [38], each neuron is assigned dedicated hardware, with each weight instantiating a separate multiplier, and all neurons operate in parallel. Fig. 3 presents a block diagram of a purely-combinational fully parallel bespoke multi-layer perceptron (MLP).

Although some studies have explored folded implementations [23], [39]–[41], sequential engines remain scarce for these technologies. While a flip-flop in CMOS technology occupies the area of approximately four NAND gates, it is equivalent to six NAND gates in EGFET technology–incurring a 50% overhead compared to CMOS. Moreover, memory options in PFE are limited and hardware-costly [1], [2]. Additionally, folded architectures rely on conventional arithmetic units, such as multipliers–which are significantly larger than their bespoke counterparts [23]–thereby limiting the potential advantages

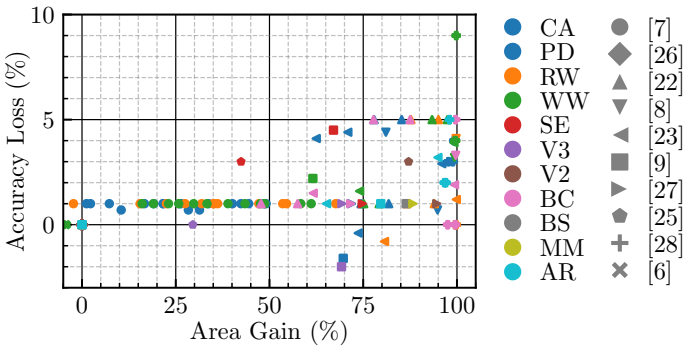

Fig. 4: Accuracy-area trade-offs among existing approaches in PFE, across commonly-used datasets.

of bespoke design. Fully parallel architectures address these issues; however, their hardware overheads might scale with model size.

2) Approximate Bespoke ML Classifiers: While bespoke implementations offer high efficiency, additional optimization is essential for more complex classifiers, as hardware overheads remain prohibitively high for practical applications [28]. Specifically targeting digital neural network classifiers, there has been a surge of research on designing approximate bespoke circuits, leveraging the perfect match formed between ML circuits and approximate computing. An overview of the current state-of-the-art achievements in approximate printed neural networks' design is illustrated in Fig. 4.

The authors in [24] demonstrated that in bespoke neural networks, the classifier's hardware overheads are closely related to the values of the model's coefficients. To exploit this correlation, [24], [25] proposed a post-training approximation technique in which model weights are strategically replaced with hardware-friendly alternatives, enabling more area-efficient bespoke multipliers. Specifically, replacing weights with nearby values (e.g., within ± 4) and balancing positive and negative replacements results in 28% area reduction for negligible accuracy loss [24]. To enable more aggressive hardware-friendly weight selection, [26] integrated this concept into the training process itself, incorporating the hardware cost of bespoke multipliers as a regularization term. This co-design strategy optimizes both model accuracy and area efficiency. Indicatively, for only up to 2% accuracy loss, 3.8x lower area can be achieved compared to the exact bespoke design [26].

Despite the significant efficiency gains in [26], [28] found that multipliers (even hardware-friendly) still require considerable area in many cases. To address this, [28] leveraged the fact that in bespoke circuits, multiplication by a power of two can be implemented through simple rewiring. By restricting model weights to power-of-two values, [28] completely eliminated the need for multipliers and further optimized the design by addressing the remaining bottleneck, i.e., additions, through adder-tree pruning. Building on this idea, [27] integrated all applied approximations directly into a genetic-based training process, in which a fine-grained bit-level pruning of input features is implemented. Compared to the exact bespoke implementation, eliminating multipliers results in 2.5x to 5x

TABLE II: Natively flexible digital bespoke ML classifiers

Ref.	Tech.	ML Classifier	Approx.	Acc. Loss	Analog-Digital Interfacing
[35]	FlexIC	Custom GNB*	-	-	5b ADCs
[34]	FlexIC	BNN	-	-	5b ADCs
[36]	FlexIC	WNN	-	-	ADCs (est. $\geq$8b)
[42]	FlexIC	MLP	In-train: pow2 weights & Ax.ADC	<5%	pruned 4b Binary ADCs
[23]	EGFET	DT, SVM	-	-	Not Reported
[39]	EGFET	SVM	-	-	4b ADCs
[24]	EGFET	MLP, SVM	Post-train: Ax.Mult & Gate-pruning	<2%	4b ADCs
[25]	EGFET	MLP, SVM	Post-train: Ax.Mult & Gate-pruning & VOS	<2%	4b ADCs
[26]	EGFET	MLP	In-train: Ax.Mult Post-train: Ax.Add	<2%	4b ADCs
[37]	EGFET	DT	Post-train: Ax.Compare	<1%	4b ADCs
[38]	EGFET	MLP	Neural Minimization	<2%	4b ADCs
[28]	EGFET	MLP	In-train: pow2 weights Post-train: Ax.Add & Ax.Relu	<5%	4b ADCs
[27]	EGFET	MLP	In-train: pow2 weights & Ax.Add	<5%	4b ADCs
[33]	EGFET	TNN	Post-train: Ax.Popcount	<1%	1b ADCs
[31]	EGFET	DT	In-train: Ax.ADC	<1%	pruned 4b Flash ADCs
[32]	EGFET	MLP	In-train: pow2 weights & Ax.ADC	<5%	pruned 4b Flash ADCs

* Gaussian Naïve Bayes.

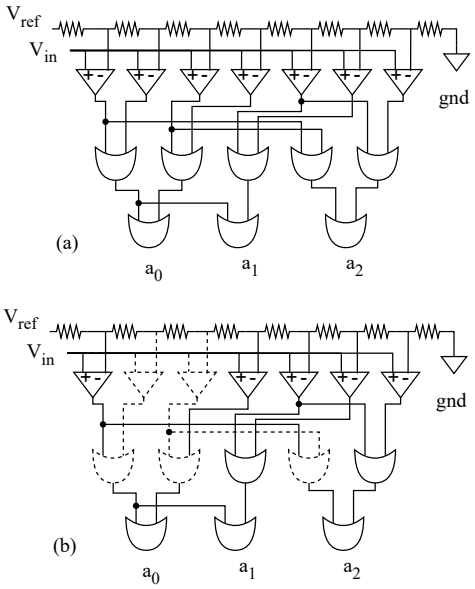

Fig. 5: Schematics of (a) 3-bit Flash ADC [32], and (b) its bespoke pruned counterpart [42].

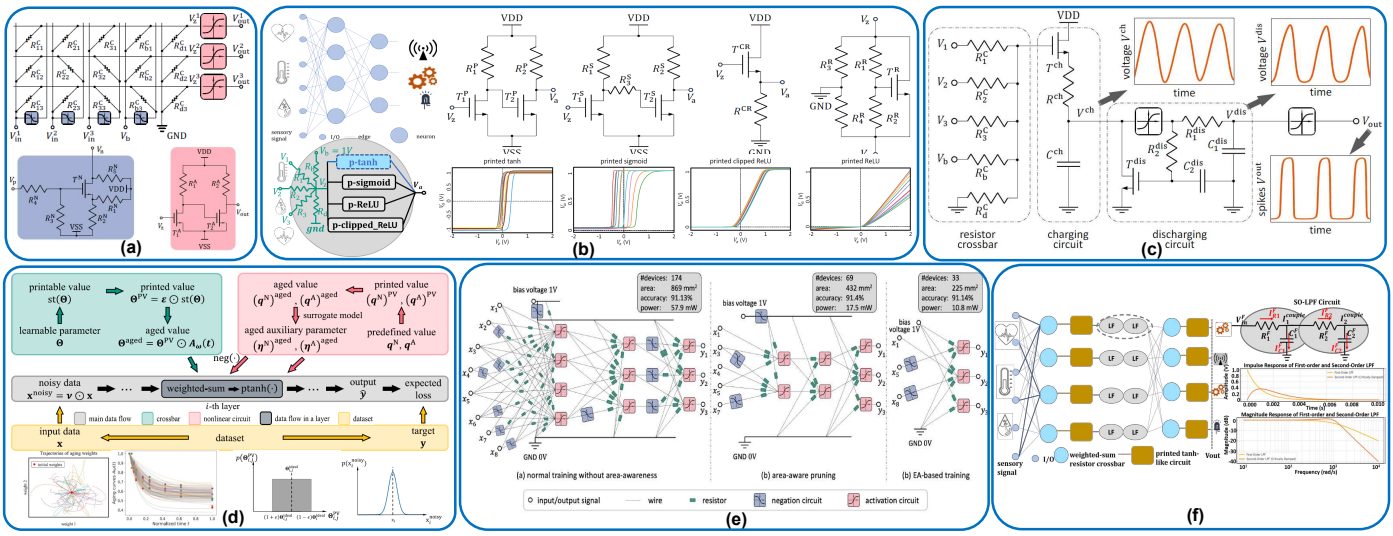

Fig. 6: (a) Schematic of an exemplary printed neuron, negative weight circuit and tanh circuit. (b) Overview of neural architecture search using four different activation functions (tanh, sigmoid, clipped ReLU, ReLU). (c) Printed spiking neuromorphic circuit. (d) Dataflow in the dependability-aware training for pNCs. (e) Area-aware training and evolutionary-based training of a pNC. (f) Overview of an adaptive second-order low-pass filter based pNC for temporal data processing.

area reduction for 1.25% average accuracy loss [28], while the approximation-aware training achieves 181x average area reduction with less than 5% accuracy loss [27]. Further maximizing hardware efficiency, [33] proposed a multiplier-less inference approach by utilizing only 1-bit inputs and ternary weights while approximating the remaining additions through approximate popcount units generated via Cartesian genetic programming. This approximation delivers a 2x area reduction compared to [27] while maintaining comparable accuracy.

Since most printed and flexible classification systems process sensor-based inputs, a significant portion of the system's area may be occupied by the mandatory ADCs. To address this, researchers extended the bespoke design paradigm to ADC design as well [31], [32], [42]. Bespoke ADC design is implemented by keeping the bare minimum representations required for each sensor and eliminating redundant circuitry. Examples of bespoke ADCs are shown in Fig. 5. At the cost of some accuracy degradation, [31], [32], [42] introduced in-training optimizations for fully-tailored ADCs, customized per input and model, resulting in substantial interfacing efficiency improvements. For example, for 1% accuracy loss, ADC costs in [32] are reduced by 8x.

C. Domain-specific Analog Processing Elements

The development of domain-specific analog processing elements is a critical area within PFE, particularly for applications demanding low cost, flexibility, and biocompatibility that traditional silicon-based electronics often cannot meet. Flexible neuromorphic [43], [44] and Printed neuromorphic circuits (pNCs) have emerged as a promising solution for such applications, drawing inspiration from the operational principles of artificial neural networks (ANNs) and spiking neural networks (SNNs) to perform computational tasks directly in the analog domain. This analog processing capability is particularly advantageous, as it eliminates the need for costly ADCs, thereby reducing device count and power consumption,

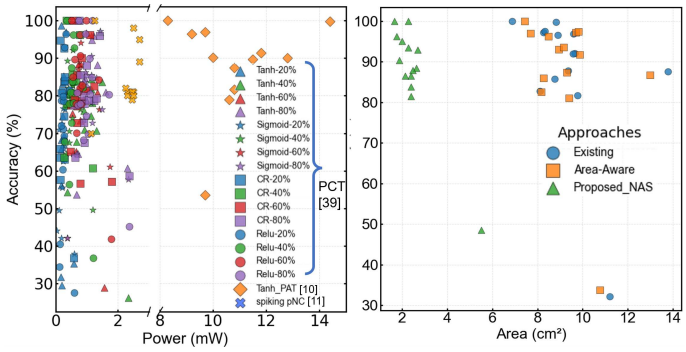

Fig. 7: Accuracy-power-area trade-offs among existing analog pNCs for different datasets [45]–[49].

which are critical constraints in many target applications. These pNCs can be categorized into three key groups according to their specific functionalities and characteristics, as described below.

1) Energy-Efficient pNCs: These circuits are specifically designed for minimal power consumption, addressing the stringent power budgets typical of printed electronics applications. Resistor crossbars are employed to emulate weighted-sum operations, a core function in neural networks. As shown in Fig. 6 (a)-(b), tanh-like activation circuits and other analog nonlinear circuits implement essential nonlinear activation functions, allowing the processing of complex data patterns with minimal power consumption [45]. Additionally, spiking neuromorphic circuits [46] (spiking pNCs, see Fig. 6(c)), which emulate biological neuron behavior by using discrete spikes to process information, significantly enhance energy efficiency. Power-aware training methodologies are integrated into the design process to explicitly consider the energy consumption of individual circuit primitives, ensuring operation within strict power constraints [47] typically imposed by printed batteries or energy harvesting systems. An overview of the current state-of-the-art achievements in area-power-accuracy tradeoff is illustrated in Fig. 7.

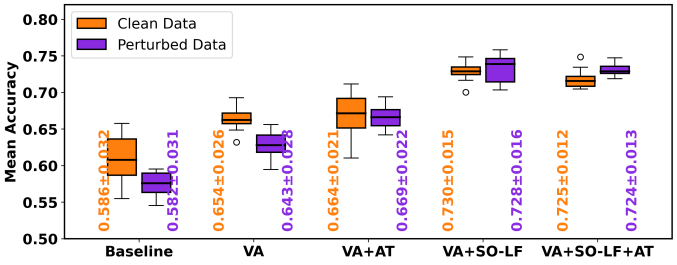

Fig. 8: Average accuracy comparison between variation-aware (VA), augmented training (AT), second-order learnable filters (SO-LF), and VA+SO-LF+AT with baseline [51] using an ablation study [52].

2) Bespoke pNCs: This category emphasizes highly customized designs, where the circuit architecture and component parameters are optimized specifically for particular datasets and application requirements. Such customization includes detailed parameterization of nonlinear components like activation functions and inverter-based circuits for negative weight operations [48], [50] as shown in Fig. 6(b). Algorithms such as neural evolutionary architecture search [48] and network pruning [49] (see Fig. 6(e)) are employed to achieve compact, area-efficient circuit designs, minimizing device counts and ensuring optimal performance tailored explicitly to the application's unique requirements.

3) Temporal Processing pNCs: These circuits as shown in Fig. 6(f), specialize in handling temporal sensory data by integrating learnable filters [51], [52] into printed temporal processing blocks (pTPBs). These blocks introduce time-dependent components, such as capacitors, to retain and process information from previous time steps. This temporal processing capability is crucial for applications like stress detection, where accurately capturing and analyzing temporal dynamics is essential. Fig. 8 presents an accuracy overview of temporal datasets [53], using an ablation analysis along with augmented training and second-order filters. Variation-aware training models process-level variations during circuit optimization, while "clean" and "perturbed" data refer to ideal and noise-augmented inputs used to evaluate robustness.

V. Robustness and Reliability

To address the manufacturing variation and reliability challenges of pNCs, various robustness-aware training methodologies have been developed that integrate the effects of manufacturing variations [48], [50], aging [54], reliability [48], [50] and sensing uncertainty [4] into the design process. As shown in Fig. 8, variation-aware training techniques aim to enhance the resilience of printed and flexible circuits by explicitly modeling and accounting for the statistical variations in component values during the training phase, allowing the network to learn parameters that are less sensitive to these variations. Similarly, aging-aware training methodologies focus on optimizing the initial parameters of pNCs by anticipating the degradation of their components over time, aiming to maintain acceptable levels of accuracy and performance throughout the expected lifetime of the device.

Dependability-aware training [4] represents a more comprehensive approach that simultaneously considers the impact of

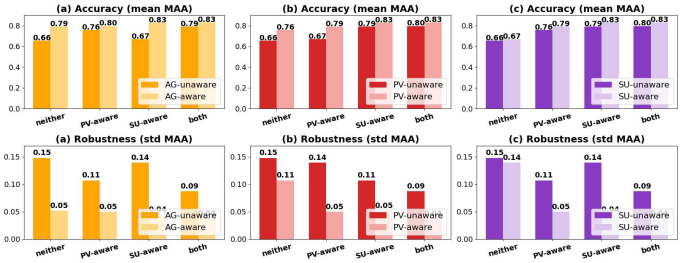

Fig. 9: Combined effects of aging (AG), printing variation (PV), and sensing uncertainty (SU) on accuracy in the dependability-aware training of pNCs. (MAA:measuring-aware accuracy) [4].

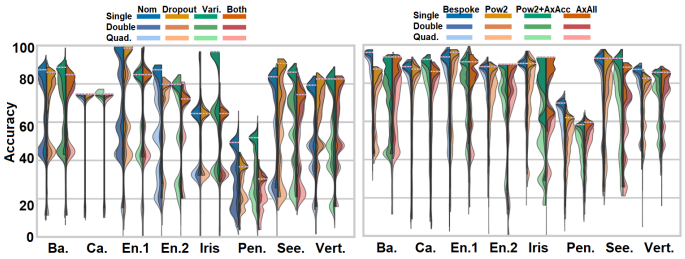

Fig. 10: Evaluation of fault sensitivity w.r.t design approaches in analog pNCs and design architectures in digital pNCs [55].

TABLE III: Comparison of Gradient-based Algorithm and Random Search for automatic test input generation.

Dataset	Faults[1]			Gradient Based		Random Pattern	
	All	+Cluster	+Untest. Removal	Fault Cov.[2]	Vec[3]	Fault Cov.[2]	Vec[3]
AcuteInfl	362	220	123 (2.94x)	93.50%	115	47.96%	59
BreastCanc	434	265	128 (3.39x)	99.22%	127	49.22%	63
EnergyY2	432	267	214 (2.02x)	97.66%	209	71.96%	154
Iris	336	207	154 (2.18x)	97.40%	150	67.53%	104
Pendigits	778	506	448 (1.74x)	98.21%	440	78.79%	32
Seeds	408	252	201 (2.03x)	96.52%	194	72.64%	146
TicTacToe	434	265	153 (2.84x)	86.27%	132	60.13%	92
VertCol2	362	220	180 (2.01x)	69.44%	125	40.00%	72
VertCol3	384	237	124 (3.1x)	99.19%	123	69.35%	86
Average	**436.7**	**271.0**	**191.7 (2.3x)**	**93.05%**	**179.4**	**61.95%**	**89.83**

[1] Faults: Total faults before and after clustering, and after clustering + untestable removal, [2] Fault Cov.: Fault Coverage (%), [3] Vec: Number of Test Vectors.

sensing uncertainty, printing variations, and aging, striving to design circuits that are robust against a combination of these factors, as shown in Fig. 9. Data augmentation techniques, including frequency domain augmentation, random cropping, jittering, time warping, and magnitude scaling, are also employed [52] (see Fig. 8) to improve the model's adaptability and robustness to noisy sensory inputs and physical variations encountered in real-world scenarios. Moreover, understanding the impact of potential defects on the functionality of printed circuits is crucial for ensuring reliability. Fault sensitivity analyses of both analog pNCs and digital pNCs are being performed at both circuit and algorithmic levels to evaluate how catastrophic faults in transistors and resistors (such as stuck-open and stuck-short faults) can affect their classification accuracy [55], as can be observed in Fig. 10. To facilitate the detection of such faults and ensure reliable operation, an

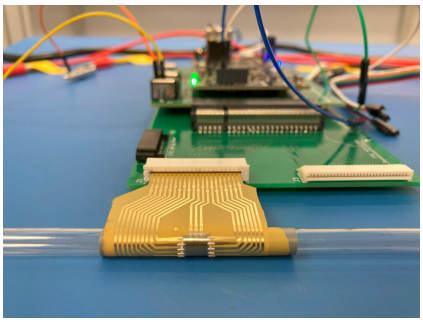

Fig. 11: Flex-RV bent in a tensile mode while executing an application.

automatic test pattern generation (ATPG) framework has been developed, specifically tailored for pNCs [56]. This framework aims to generate efficient test inputs that can maximize the output discrepancies between fault-free and faulty circuits, enabling comprehensive fault detection with a reduced number of test vectors. As shown in Table III, the gradient-based method significantly improves fault coverage and testing efficiency for analog pNCs, achieving over 90% fault coverage across datasets, outperforming random pattern testing. Additionally, we observe how fault abstraction significantly reduced the fault space (e.g., by 3.39× in *BreastCanc*). However, datasets with complex fault behaviors, such as *TicTacToe* and *VertCol2*, remain challenging, often causing optimization to get stuck in local optima and thus require extra iterations for better coverage. These collective efforts in robustness-aware design, fault analysis, and test generation are essential steps towards establishing the dependability of printed analog processing elements and enabling their widespread and reliable use in various emerging applications.

Flexible electronic components endure significant mechanical stress when they are bent. Thus, it is important to measure their mechanical strain in the form of bendability tests, in order to accurately assess their reliability and flexibility range in real-world deployment scenarios. There have been many studies which perform parametric and functional tests at device level (TFT, electrodes etc.) under static and dynamic bending conditions [57]–[59]. The first study to demonstrate the bendability beyond device or a basic circuit level is Flex-RV [2], the 32-bit RISC-V processor fabricated as a FlexIC described in Section IV-A, which is assembled on a flexible PCB (FlexPCB). The bendability of Flex-RV under tensile and compressive strains has been validated through real application execution, as illustrated in Fig. 11. The results demonstrate that Flex-RV on a FlexPCV remains fully functional when bent to a 3 mm radius of curvature, exhibiting only minor performance variations depending on the applied bending strain.

VI. Conclusion

Printed and flexible electronics offer a promising alternative to silicon-based technologies for low-cost, lightweight, and conformal applications, despite challenges in integration density, device variability, and circuit complexity. Domain-specific circuits are enabled through extreme customizations–supported by the underlying technologies–while natively flexible general-purpose processors have been successfully fabricated and tested on flexible substrates and PCBs. Reliability has been improved through variation- and aging-aware training, fault sensitivity analysis, and dedicated test generation. Together, these developments show that printed and flexible systems can achieve competitive levels of hardware efficiency and robustness. Continued algorithm-hardware co-design and System Technology Co-Optimization (STCO) for printed and flexible electronics remain essential to scale these technologies for practical, real-world deployment.

Acknowledgment

This work is supported by the European Research Council (ERC) and co-funded by the H.F.R.I call “Basic Research Financing (Horizontal support of all Sciences)” under the National Recovery and Resilience Plan “Greece 2.0” (H.F.R.I. Project Number: 17048).

References

[1] N. Bleier, M. Mubarik, F. Rasheed, J. Aghassi-Hagmann, M. B. Tahoori, and R. Kumar, “Printed microprocessors,” in *Annual International Symposium on Computer Architecture (ISCA)*, 2020, pp. 213–226.

[2] E. Ozer *et al.*, “Bendable non-silicon risc-v microprocessor,” *Nature*, pp. 1–6, 2024.

[3] J. Henkel *et al.*, “Approximate computing and the efficient machine learning expedition,” in *International Conference On Computer Aided Design (ICCAD)*, 2022, pp. 1–9.

[4] H. Zhao, M. Hefenbrock, M. Beigl, and M. B. Tahoori, “Highly-dependable printed neuromorphic circuits based on additive manufacturing,” *Flexible and Printed Electronics*, vol. 8, no. 2, p. 025018, 2023.

[5] F. Rasheed, M. Hefenbrock, M. Beigl, M. B. Tahoori, and J. Aghassi-Hagmann, “Variability modeling for printed inorganic electrolyte-gated transistors and circuits,” *IEEE transactions on electron devices*, vol. 66, no. 1, pp. 146–152, 2018.

[6] Pragmatic, “Flexic Platform Gen3,” https://www.pragmaticsemi.com/foundry/flexic-platform-gen-3, 2025.

[7] T. Takayama *et al.*, “A CPU on a plastic film substrate,” in *Symposium on VLSI Technology*, 2004, pp. 230–231.

[8] H. Dembo *et al.*, “RFCPUs on glass and plastic substrates fabricated by TFT transfer technology,” in *IEEE International Electron Devices Meeting (IEDM)*, 2005, pp. 125–127.

[9] N. Karaki, T. Nanmoto, H. Ebihara, S. Utsunomiya, S. Inoue, and T. Shimoda, “A flexible 8b asynchronous microprocessor based on low-temperature poly-silicon TFT technology,” in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2005, pp. 272–273.

[10] Y. Kurokawa *et al.*, “UHF RFCPUs on flexible and glass substrates for secure RFID systems,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 292–299, 2008.

[11] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, “An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 284–291, 2012.

[12] K. Myny *et al.*, “8b thin-film microprocessor using a hybrid oxide-organic complementary technology with inkjet-printed P^2ROM memory,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 486–487.

[13] J. Biggs *et al.*, “A natively flexible 32-bit arm microprocessor,” *Nature*, vol. 595, no. 7868, pp. 532–536, 2021.

[14] H. H Çeliker, A. Sou, B. Cobb, W. Dehaene, and K. Myny, “Flex6502: a flexible 8b microprocessor in 0.8 μm metal-oxide thin-film transistor technology implemented with a complete digital design flow running complex assembly code,” in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 65, 2022, pp. 272–274.

[15] N. Bleier, C. Lee, F. Rodriguez, A. Sou, S. White, and R. Kumar, “Flexicores: Low footprint high yield field reprogrammable flexible microprocessors,” in *Annual International Symposium on Computer Architecture (ISCA)*, 2022, pp. 831–846.

[16] H. Çeliker, W. Dehaene, and K. Myny, "Multi-project wafers for flexible thin-film electronics by independent foundries," *Nature*, vol. 629, p. 335–340, 2024.

[17] Z. Cui, *Printed electronics: materials, technologies and applications*. John Wiley & Sons, 2016.

[18] J. S. Chang, A. F. Facchetti, and R. Reuss, "A circuits and systems perspective of organic/printed electronics: review, challenges, and contemporary and emerging design approaches," *IEEE Journal on emerging and selected topics in circuits and systems*, vol. 7, no. 1, pp. 7–26, 2017.

[19] C. Marques *et al.*, "Progress Report on "From Printed Electrolyte-Gated Metal-Oxide Devices to Circuits"," *Advanced Materials*, vol. 31, 2019.

[20] T.-J. Chang, Z. Yao, P. J. Jackson, B. P. Rand, and D. Wentzla, "Architectural tradeoffs for biodegradable computing," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, 2017, pp. 706–717.

[21] E. Ozer *et al.*, "Bespoke machine learning processor development framework on flexible substrates," in *Int. Conf. Flexible and Printable Sensors and Systems (FLEPS)*, 2019, pp. 1–3.

[22] K. Iordanou *et al.*, "Low-cost and efficient prediction hardware for tabular data using tiny classifier circuits," *Nature Electronics*, vol. 7, no. 5, pp. 405–413, May 2024.

[23] M. H. Mubarik *et al.*, "Printed machine learning classifiers," in *Annu. Int. Symp. Microarchitecture (MICRO)*, 2020, pp. 73–87.

[24] G. Armeniakos, G. Zervakis, D. Soudris, M. B. Tahoori, and J. Henkel, "Cross-layer approximation for printed machine learning circuits," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2022, pp. 190–195.

[25] G. Armeniakos, G. Zervakis, D. Soudris, M. B. Tahoori, and J. Henkel, "Model-to-circuit cross-approximation for printed machine learning classifiers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 42, no. 11, pp. 3532–3544, 2023.

[26] G. Armeniakos, G. Zervakis, D. Soudris, M. B. Tahoori, and J. Henkel, "Co-design of approximate multilayer perceptron for ultra-resource constrained printed circuits," *IEEE Trans. Comput.*, pp. 1–8, 2023.

[27] F. Afentaki, M. Hefenbrock, G. Zervakis, and M. B. Tahoori, "Embedding hardware approximations in discrete genetic-based training for printed mlps," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2024, pp. 1–6.

[28] F. Afentaki, G. Saglam, A. Kokkinis, K. Siozios, G. Zervakis, and M. B. Tahoori, "Bespoke approximation of multiplication-accumulation and activation targeting printed multilayer perceptrons," in *International Conference on Computer Aided Design (ICCAD)*, 2023, pp. 1–9.

[29] D. D. Weller *et al.*, "Printed stochastic computing neural networks," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, 2021, pp. 914–919.

[30] A. Kokkinis, G. Zervakis, K. Siozios, M. B. Tahoori, and J. Henkel, "Hardware-aware automated neural minimization for printed multilayer perceptrons," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2023, pp. 1–2.

[31] G. Armeniakos, P. L. Duarte, P. Pal, G. Zervakis, M. B. Tahoori, and D. Soudris, "On-sensor printed machine learning classification via bespoke adc and decision tree co-design," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2024, pp. 1–6.

[32] F. Afentaki, P. C. L. Duarte, G. Zervakis, and M. B. Tahoori, "Reducing adc front-end costs during training of on-sensor printed multilayer perceptrons," *IEEE Embedded Systems Letters*, vol. 16, no. 4, pp. 353–356, 2024.

[33] V. Mrazek *et al.*, "Evolutionary approximation of ternary neurons for on-sensor printed neural networks," in *International Conference on Computer Aided Design (ICCAD)*, 2024, p. 9.

[34] E. Ozer, J. Kufel, J. Biggs, J. Myers, C. Reynolds, and G. Brown, "Binary neural network as a flexible integrated circuit for odour classification," in *IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*, 2020, pp. 1–4.

[35] E. Ozer *et al.*, "A hardwired machine learning processing engine fabricated with submicron metal-oxide thin-film transistors on a flexible substrate," *Nature Electronics*, vol. 3, no. 7, pp. 419–425, 2020.

[36] V. Pillai *et al.*, "arrWNN: Arrhythmia-detecting weightless neural network flexic," in *IEEE International Flexible Electronics Technology Conference (IFETC)*, 2024, pp. 1–4.

[37] K. Balaskas, G. Zervakis, K. Siozios, M. B. Tahoori, and J. Henkel, "Approximate decision trees for machine learning classification on tiny printed circuits," in *Int. Symp. Quality Electronic Design*, 2022, pp. 1–6.

[38] A. Kokkinis, G. Zervakis, K. Siozios, M. B. Tahoori, and J. Henkel, "Enabling printed multilayer perceptrons realization via area-aware neural minimization," *IEEE Transactions on Computers*, vol. 74, no. 4, pp. 1461–1469, 2025.

[39] I. Sertaridis, S. Besias, F. Afentaki, K. Balaskas, and G. Zervakis, "Compact yet highly accurate printed classifiers using sequential support vector machine circuits," in *International Symposium on Circuits and Systems (ISCAS)*, 2025.

[40] S. Besias, I. Sertaridis, F. Afentaki, K. Balaskas, and G. Zervakis, "Late breaking results: Energy-efficient printed machine learning classifiers with sequential svms," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2025.

[41] G. Saglam, F. Afentaki, G. Zervakis, and M. Tahoori, "Sequential printed multilayer perceptron circuits for super-tinyml multi-sensory applications," in *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2025, p. 30–35.

[42] P. C. Lozano Duarte, F. Afentaki, G. Zervakis, and M. Tahoori, "Design and in-training optimization of binary search adc for flexible classifiers," in *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2025, p. 754–760.

[43] A. Lebanov *et al.*, "Flexible unipolar igzo transistor-based integrate and fire neurons for spiking neuromorphic applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 18, no. 1, pp. 200–214, 2024.

[44] M. Velazquez Lopez *et al.*, "A tunable multi-timescale indium-gallium-zinc-oxide thin-film transistor neuron towards hybrid solutions for spiking neuromorphic applications," *Communications Engineering*, vol. 3, no. 1, p. 102, Jul 2024.

[45] H. Zhao, P. Pal, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Power-Aware Training for Energy-Efficient Printed Neuromorphic Circuits," in *International Conference on Computer-Aided Design (ICCAD)*, 2023.

[46] P. Pal *et al.*, "Analog printed spiking neuromorphic circuit," in *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2024, pp. 1–6.

[47] T. Gheshlaghi, H. Zhao, P. Pal, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Power-constrained printed neuromorphic hardware training," in *2025 Design Automation Conference (DAC)*, 2025, pp. 1–6.

[48] P. Pal, H. Zhao, T. Gheshlaghi, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Neural architecture search for highly bespoke robust printed neuromorphic circuits," in *Proceedings of the 42nd IEEE/ACM International Conference on Computer-Aided Design*, 2024.

[49] H. Zhao, P. Pal, M. Hefenbrock, Y. Wang, M. Beigl, and M. B. Tahoori, "Neural evolutionary architecture search for compact printed analog neuromorphic circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–1, 2024.

[50] H. Zhao *et al.*, "Highly-Bespoke Robust Printed Neuromorphic Circuits," in *Design, Automation and Test in Europe (DATE)*. IEEE, 2023.

[51] H. Zhao, P. Pal, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Towards Temporal Information Processing–Printed Neuromorphic Circuits with Learnable Filters," in *Proceedings of the 18th ACM International Symposium on Nanoscale Architectures*, 2023, pp. 1–6.

[52] T. Gheshlaghi, P. Pal, H. Zhao, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Adapt-pnc: Mitigating device variability and sensor noise in printed neuromorphic circuits with so adaptive learnable filters," in *2025 Design Automation and Test in Europe (DATE)*, 2025, pp. 1–6.

[53] Y. Chen *et al.*, "The ucr time series classification archive," July 2015, www.cs.ucr.edu/~eamonn/time_series_data/.

[54] H. Zhao, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Aging-Aware Training for Printed Neuromorphic Circuits," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD '22)*, 2022.

[55] P. Pal *et al.*, "Fault sensitivity analysis of printed bespoke multilayer perceptron classifiers," in *2024 IEEE European Test Symposium (ETS)*, 2024, pp. 1–6.

[56] T. Gheshlaghi, P. Pal, S. Alexander, M. Hefenbrock, M. Beigl, and M. B. Tahoori, "Automatic test pattern generation for printed neuromorphic circuits," in *2025 European Test Symposium (ETS)*, 2025.

[57] T.-W. Kim, J.-S. Lee, Y.-C. Kim, Y.-C. Joo, and B.-J. Kim, "Bending strain and bending fatigue lifetime of flexible metal electrodes on polymer substrates," *Materials*, vol. 12, no. 15, 2019.

[58] H.-W. Jang, G.-H. Kim, and S.-M. Yoon, "Analysis of mechanical and electrical origins of degradations in device durability of flexible InGaZnO thin-film transistors," *ACS Appl. Electron. Mater.*, vol. 2, no. 7, p. 2113–2122, 2020.

[59] Q. Zahid H *et al.*, "Dc and ac performance of InGaZnO thin-film transistors on flexible PEEK substrate," *IEEE Transactions on Electron Devices*, vol. 71, no. 10, pp. 6073–6078, 2024.